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THE ANALYSIS OF REDUNDANT TRANSISTOR NETWORKS WITH DUPLICATION OF POWER SUPPLY IN TERMS OF RELIABILITY

Different designs with reservation of power supply are analyzed in this article. The developers of high reliable computing systems often use n-of-m reservation technique to provide fault-tolerance in a digital circuit. It is need three channels and special gate – voter (major) to traditional two-of-three reservation in most simple design. Tolerance to failures in power supply, gates and wires can be provided using of this technique at the same time triplication of voter should be used to provide tolerance to failures in voter. The authors proposed using of reservation at transistor-level in combination with n-of-m reservation because it provides more opportunities in optimization. At first, authors researched using of redundant gates in fault-tolerant computing systems, then reservation at transistor-level of pull-up and pull-down networks. In this paper, influence of power supply on a circuit reliability is analyzed and technique of reservation at transistor-level is improved.

***Key words**: reliability, fault-tolerance, reservation at transistor-level, supply voltage, triplication, n-of-m reservation, redundant gates.*

Introduction

The development of high reliable computing systems is one of the most practical-oriented field of computing science. It includes such fields as synthesis of high reliable computing systems, analysis of high reliable computing systems etc. In critical systems, high reliability is reached using fault-tolerant (FT) structures [1]. In contrast to just high reliable systems, fault-tolerant systems designed to ignore failures of its blocks. Therefore, it does not need time to reconfiguration and can provide functionality without stops [2]. Fault-tolerance often is provided as n-of-m reservation (using of n-channels and special gate – voter or major-gate) [3]. Previously Authors showed that reservation of transistors (using redundant gates) better in terms of reliability than n-of-m reservation of units or gates [4-6]. For example, the redundant gates can be demanded in radiation-tolerant digital devices for aerospace or other critical fields [7-9]. One of the previous purposes was to develop the solutions for power supply reservation in redundant gates. The set of solutions for reservation of power supply is proposed and analyzed in this paper.

1. Reservation at CMOS transistor-level

Principles of reservation at CMOS transistor-level will be described on the example of the gate that have logic function (1) [10]:

$$P(NA,NB,NC) = NB \cdot NC \vee NA \cdot (NC \vee NB), \quad (1)$$

This function provides tolerance to faults. The reliability probability of this gate can be calculated (2) using exponential model of time before failure distribution:

$$P_0 = e^{-10 \cdot \lambda \cdot t}, \quad (2)$$

where λ – failure rate;

t – time

To improve reliability by means of providing fault-tolerance relative to failures of transistors the reservation at transistor-level was proposed.

In this case, reservation is carried out as using of functionally complete tolerant (FCT) functions (3) at transistor-level, fig. 1 [11]:

$$f_i f_i \vee f_i f_i. \quad (3)$$

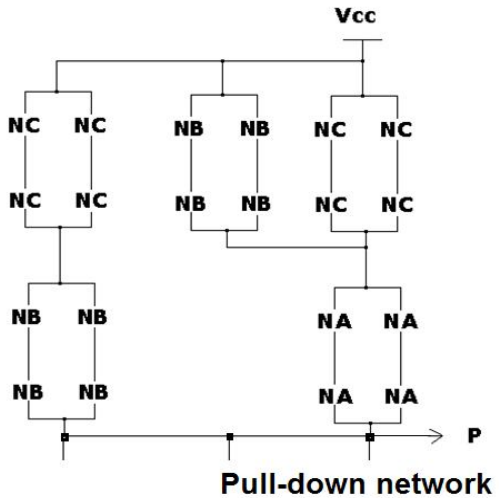

Fig. 1. Redundant major-gate schematic diagram at transistor-level using FCT-function (3)

Redundant major-gate (MG) have four time more transistors 4*10=4, speed parameter - the path from supply to output increases two time but it is normal for fault-tolerant circuits and also keeps within restriction on noise stability [12].

The logic function of redundant transistor network (RTD) will be saved in case of fault:

$$f_i f_i \vee f_i \cdot 1 = f_i, \quad (4)$$

$$f_i f_i \vee f_i \cdot 0 = f_i, \quad (5)$$

$$f_i f_i \vee f_i \cdot \bar{f}_i = f_i,\ i = 1..3. \quad (6)$$

The reliability probability of redundant major-gate ($P(t)_{ftm}$) will be equal to (7). Failure rate of transistors is equal to $\lambda=10^{-5}$ in all calculations:

$$P(t)_{ftm} = [e^{-4\cdot\lambda\cdot t} + 4\cdot e^{-3\cdot\lambda\cdot t}(1-e^{-\lambda\cdot t})]^{10}. \quad (7)$$

At the same time, FCT-functions can be applied not only to single transistors but also for a pull-up and a pull-down transistor network. In this case, many faults in one network is allowed.

Reliability probability of this redundant major-gate $P(t)_{ftm2}$ is equal to (8):

$$P(t)_{ftm2} = [e^{-20\cdot\lambda\cdot t} + 4\cdot e^{-15\cdot\lambda\cdot t}(1-e^{-5\lambda\cdot t})]^2. \quad (8)$$

Let us compare all reliability probabilities (2), (7), (8) with reliability probabilities of fault-tolerant circuits designed with use of triplication (9) and triplication with reservation of major-gate (10) to analyze it, fig.2:

$$P_3 = (3\cdot e^{-2\cdot(10)\cdot\lambda\cdot t} - 2\cdot e^{-3\cdot(10)\cdot\lambda\cdot t})\cdot e^{-(10)\cdot\lambda\cdot t}, \quad (9)$$

$$P_{33} = (3\cdot e^{-2\cdot(10)\cdot\lambda\cdot t} - 2\cdot e^{-3\cdot(10)\cdot\lambda\cdot t})\times (3\cdot e^{-2\cdot(10)\cdot\lambda\cdot t} - 2\cdot e^{-3\cdot(10)\cdot\lambda\cdot t}). \quad (10)$$

It can be seen that triplication P_3(3*10+10=40 transistors) worse than circuit without redundancy P_0 (10 transistors). The P_{33} better than initial circuit but have maxmimum complexity 3*10+3*10=60 transistors. The best reliability probability have P_{ftm} (10*4=40 transistors). The P_{ftm2} and P_{33} are approximately equal in time interval [0,4000] but become worse than initial circuit in time interval [5000,8000], fig. 3.

Redundancy at transistor-leve $P_{ftm}(t)$ shows best reliability. It happens because redundancy is used at the lowest level of each single transistor. In fact it is a lowest level of circuit design. Thus, as a hypothesis, the further increasing of reliability can be achieved only by using of new technologies for transistors. The price of reliability is performance, energy consumption and complexity. In [6] authors showed that transistor-level reservation better than triplication from the point of view of energy-consumption in spite of the fact that it use more transistors in certain cases.

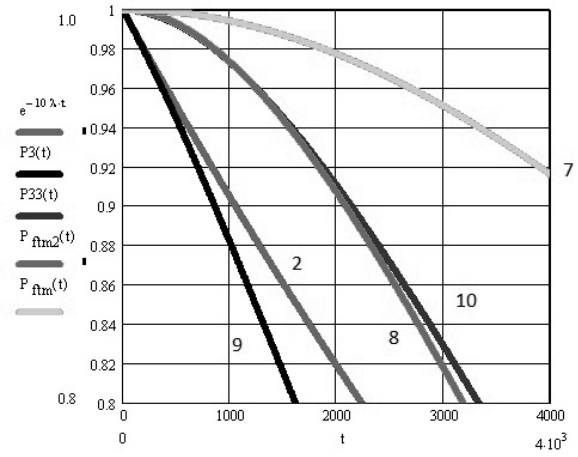

Fig.2.The reliability probability comparison of MG designed in different FT techniques

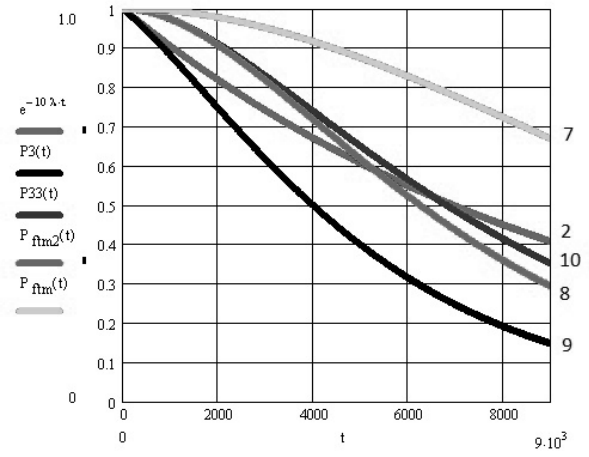

Fig.3.The reliability probability comparison of MG designed in different FT techniques

2. Reservation at CMOS transistor-level with power supply duplication

Power supply can be reserved in n-of-m fault-tolerant structures as each channel can have its own source. Let us improve proposed technique of fault-tolerant designing by adding possibilities of power supply reservation.

Use of FCT-functions is replacement of a single transistor by RTD. Each RTD have two inputs, it are sources of CMOS transistors, and one output, it is connected drains of CMOS transistors. Therefore, we

can use redundant source of CMOS transistor to connect redundant power supply, fig. 4.

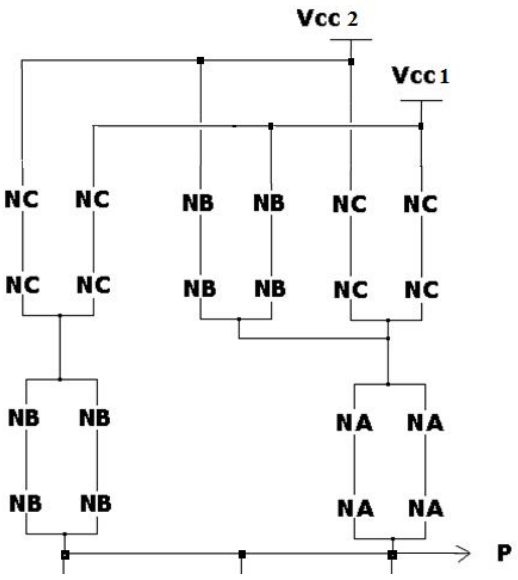

Fig. 4. Redundant MG schematic diagram at transistor-level using FCT-function (3) with duplication of power supply

This improvement allows providing tolerance to failures in one power supply source. It does proposed technique of fault-tolerant designing be equal to two-of-three redundancy. Complexity of power supply will be set to 100 λ. Thus, reliability probability taking into account reliability of power supply can be calculated as (11), (12), (13) and (14):

$$P(t)_{ftm} = [e^{-4\cdot\lambda\cdot t} + 4\cdot e^{-3\cdot\lambda\cdot t}(1-e^{-\lambda\cdot t})]^7 \times \times (1\text{-}(1-e^{-106\lambda\cdot t})^2), \quad (11)$$

$$P(t)_{ftm2} = [e^{-20\cdot\lambda\cdot t} + 4\cdot e^{-15\cdot\lambda\cdot t}(1-e^{-5\lambda\cdot t})]^1 \times \times (1\text{-}(1-e^{-120\lambda\cdot t})^2), \quad (12)$$

$$P_3 = (3\cdot e^{-2\cdot(110)\cdot\lambda\cdot t} \text{-} 2\cdot e^{-3\cdot(110)\cdot\lambda\cdot t})\cdot e^{-(110)\cdot\lambda\cdot t}, \quad (13)$$

$$P_{33} = (3\cdot e^{-2\cdot(110)\cdot\lambda\cdot t} \text{-} 2\cdot e^{-3\cdot(110)\cdot\lambda\cdot t}) \times \times (3\cdot e^{-2\cdot(110)\cdot\lambda\cdot t} \text{-} 2\cdot e^{-3\cdot(110)\cdot\lambda\cdot t}). \quad (14)$$

To analyze received reliability probability the functions graphs should be presented, fig.5.

Correct operation cannot be guaranteed if failures in transistors and power supply occurs in one time. Thus, reduced redundant networks can be used to provide tolerance to failures of power supply without tolerance to failures of transistors. The complexity of such solution is equal to 150% of initial circuit complexity.

It use two pull-up networks and one pull-down network because GND power supplies can be joint. The correct work of this circuit was proved by simulation in CAD NI MultiSim. This reservation will be better if reliability of a power supply much worse in comparison with reliability of logic circuit, fig. 6.

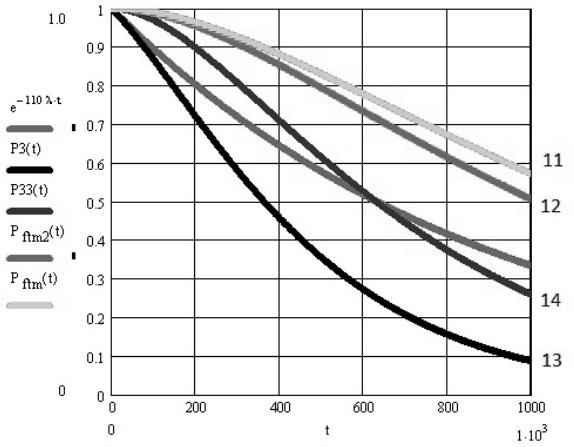

Fig. 5. The reliability probability comparison of MG designed in different FT techniques taking into account reliability of power supply

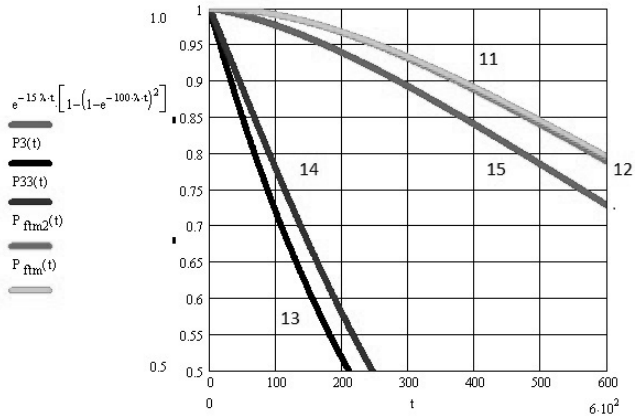

Fig. 6. The reliability probability comparison of MG designed in different FT techniques taking into account reliability of power supply

Duplication (15) of power supply not much worse than reservation at transistor-level:

$$e^{-15\lambda\cdot t}(1\text{-}(1-e^{-100\lambda\cdot t})^2. \quad (15)$$

It happens because complexity of power supply much more complexity of circuit. Let us reduce complexity of power supply from 100 λ to 10 λ and see how it will influence on reliability, fig. 7.

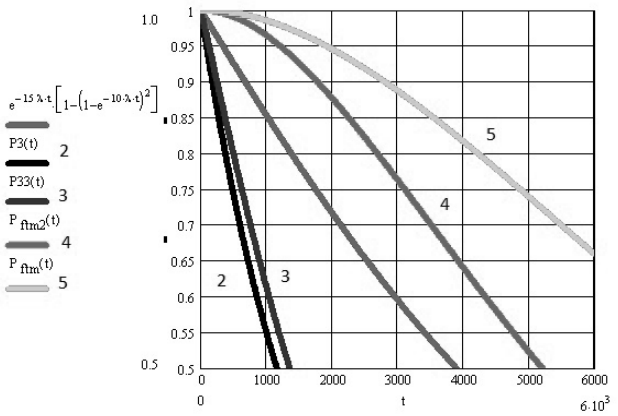

Fig.7.The reliability probability comparison of MG designed in different FT techniques taking into account reliability of power supply

We can see that reservation at transistor-level still much better than all other solutions. Circuit with power source duplication better in terms of reliability than two-of-three redundant circuit. Thus, in certain cases reliability can be increased using only 50% increase complexity. Let us see, is it possible to provide tolerance to failures in power supply at the same time with tolerance to failures in transistors?

Circuit can be protected from multiple stuck-at faults with help of redundancy at transistor-level using FCT-functions. In one case, it will be FCT-functions for more variables but in another, it can be simple duplication of transistor networks. It demands 800% redundancy but it can be reduced using only one pull-down network. In this case, the reliability probability will become equal to (16), (17):

$$P(t)_{ftm} = [e^{-4\cdot\lambda\cdot t} + 4\cdot e^{-3\cdot\lambda\cdot t}(1-e^{-\lambda\cdot t})]^5 \times \times (1-(1-e^{-100\lambda\cdot t}\cdot[e^{-4\cdot\lambda\cdot t} + 4\cdot e^{-3\cdot\lambda\cdot t}(1-e^{-\lambda\cdot t})]^5)^2), \quad (16)$$

$$P(t)_{ftm2} = [e^{-20\cdot\lambda\cdot t} + 4\cdot e^{-15\cdot\lambda\cdot t}(1-e^{-5\lambda\cdot t})]^1 \times \times (1-(1-e^{-120\lambda\cdot t}\cdot[e^{-20\cdot\lambda\cdot t} + 4\cdot e^{-15\cdot\lambda\cdot t}(1-e^{-5\lambda\cdot t})])^2). \quad (17)$$

Let see how it influence on reliability probability of circuit. In figure 8, reliability probability of power supply is equal to 10 λ.

Conclusions

The designers of critical systems in which reliability has to be guaranteed without using time to repair (reconfiguration) can use only passively fault-tolerant designing techniques. Nowadays, n-of-m reservation is most popular solution for such systems but development of digital technologies allows using new techniques. One of them it is use of redundant gates with redundancy at transistor-level. Previously we showed that use of redundant gates better than the deep two-of-three reservation in reliability, complexity and in certain cases performance but without taking into account reliability of power supply. Advantages and prospects of using redundant gates are shown in this paper. Summing up results, we can say that reservation at transistor-level it is a best alternative to traditional n-of-m reservation in the view of fault-tolerant designing. The development of digital technologies gives interesting opportunities; such parameters as performance, energy-consumption, and reliability become priority at the same time complexity stops being such significant [13, 14]. Therefore, in future designers of high-reliable computing systems will be able to use gates that are more redundant. For example, fault-tolerant structure with nine transistors.

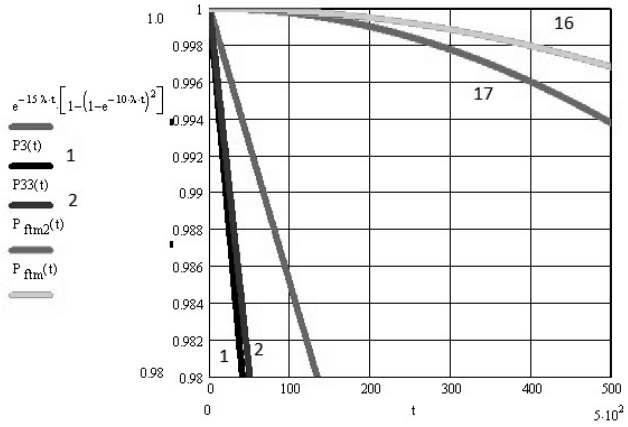

Fig.8.The reliability probability comparison of MG designed in different FT techniques taking into account reliability of power supply

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АНАЛИЗ НАДЕЖНОСТИ ИЗБЫТОЧНЫХ ТРАНЗИСТОРНЫХ СЕТЕЙ С ДУБЛИРОВАНИЕМ ИСТОЧНИКА ПИТАНИЯ

А. Н. Каменских, С. Ф. Тюрин

В статье анализируются различные проекты отказоустойчивых проектов с резервированием источника питания. Разработчики высоконадежных вычислительных систем часто используют мажоритарное резервирование для обеспечения отказоустойчивости в цифровых схемах. Оно требует три канала и мажоритарный элемент в классическом трехканальном резервировании, которое обеспечивает устойчивость к отказам в источнике питания, логических элементах схемы и соединениях. Однако, необходимо резервировать мажоритарные элементы, чтобы обеспечить полную отказоустойчивость. Авторы предлагают использование резервирования на транзисторном уровне в комбинации с мажоритарным резервированием, что позволяет лучше оптимизировать получаемые схемы. В начале, было исследовано применение элементов с избыточным базисом в высоконадежных вычислительных системах, затем резервирование транзисторных сетей. В этой статьи исследуется влияние источника питания на надежность вычислительной системы и способы резервирования источника питания в избыточных транзисторных структурах.

Ключевые слова: надежность, отказоустойчивость, резервирование на транзисторном уровне, источник питания, троирование, мажоритарное резервирование, логические элементы с избыточным базисом.

АНАЛІЗ НАДІЙНОСТІ НАДЛИШКОВИХ ТРАНЗИСТОРНИХ МЕРЕЖ З ДУБЛЮВАННЯМ ДЖЕРЕЛА ЖИВЛЕННЯ

А. М. Каменських, С. Ф. Тюрін

У статті аналізуються різні проекти відмовостійких проектів з резервуванням джерела живлення. Розробники високонадійних обчислювальних систем часто використовують мажоритарне резервування для забезпечення відмовостійкості в цифрових схемах. Воно потребує три канали і мажоритарний елемент в класичному трьохканальному резервування, яке забезпечує стійкість до відмов в джерелі живлення, логічних елементах схеми і з'єднаннях. Однак, необхідно резервувати мажоритарні елементи, щоб забезпечити повну відмовостійкість. Автори пропонують використовувати резервування на транзисторному рівні в комбінації з мажоритарним резервуванням, що дозволяє краще оптимізувати одержувані схеми. На початку, було досліджено застосування елементів з надмірним базисом в високонадійних обчислювальних системах, потім резервування транзисторних мереж. У цій статті досліджується вплив джерела живлення на надійність обчислювальної системи і способи резервування джерела живлення в надлишкових транзисторних структурах.

Ключові слова: надійність, відмовостійкість, резервування на транзисторному рівні, джерело живлення, троювання, мажоритарне резервування, логічні елементи з надмірним базисом.

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