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FAULT TOLERANT LOGIC ELEMENT - FTLUT FPGA

In the article according to concept of the functionally complete tolerant element (FCT) it is proposed fault tolerant LUT (Look up table) FPGA. The FCT element (logic element with the redundancy basis) retain functional completeness in case faults. FCT element allows to perform FPGA self-repair after faults. The article discusses the advantage of the quadrupling of the LUT 's transistors in comparison with the tripling in a number of cases. It appears to be more preferable on the reliability function, than tripling, moreover expenditure for this - order 30%, that not too it is much in comparison with a multiple increase in the equipment during the introduction of additional channels.

Keywords: *Basis function, Faults, Fault tolerance, Majority element, Redundancy, Reliability.*

Introduction

A field-programmable gate array (FPGA) consists of an array of logic blocks (Configurable Logic Block, CLB) [1-7]. CLB consists of a few logical elements or cells (LE). A typical cell consists of a 4-input LUT (Look Up Table). It is the tree of the MOS transistors – Fig.1:

In the SRAM cells loads the truth table of the required logical function. They are usually used LUT on 4,5 variables, they already adapt LUT to 6 and even on 7 variables. To Fig.1 is depicted LUT to 4 input variables A, B, C, D. As is known, the classical fault models in digital circuits include [8,9] Line faults (Stuck-at fault: stuck-at-0, for example $\mathbf{D^0}$, stuck-at-1, for example $\mathbf{D^1}$), Transistor faults (stuck -short or stuck-on, stuck-open or stuck-off), Bridging Faults: Dominant; Wired AND, OR; Dominant AND/ OR.

It is shown [10, 11], that with the fault of any one transistor, or lines, except transistors in the output inverter, during the appropriate reconfiguration, it is possible to use this LUT, but on n -1 variable - Table. 1.

However, last inverter in the tree of the transmitting transistors, "spoils" entire picture. Any fault of one of two transistors leads to the impossibility of restoration, i.e. it leads to the failure of entire LUT. This "bottleneck", "needle ear" through which cannot in the critical situation pass entire enormous functionality this LUT-4 65536 possible realizable functions!

The article describes the proposed methods of increasing the reliability of the logic elements.

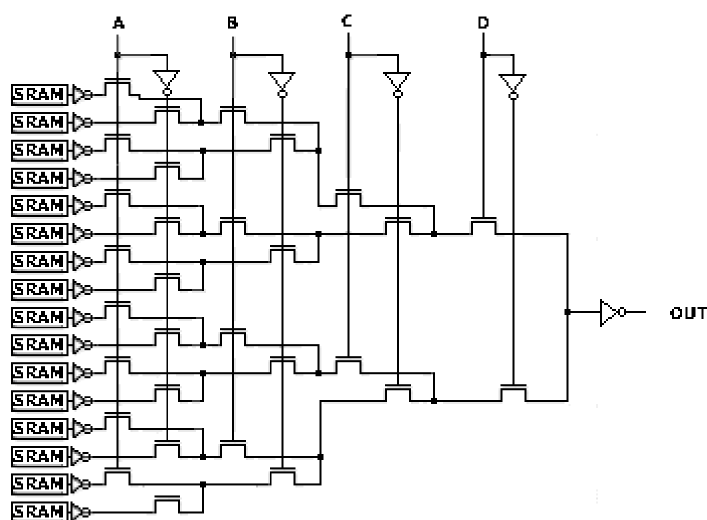

Fig. 1. Logic element - a 4-input LUT FPGA (multiplexer 16-1, the tree of the 30-MOS transistors)

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Table 1

The n -1 LUT for 4 LUT with the fault of any one transistor, or lines, except transistors in the output inverter

D	C	B	A	No faults	D^0	D^1	C^0	C^1	B^0	B^1	A^0	A^1
0	0	0	0	0	0	8	0	4	0	2	0	1
0	0	0	1	1	1	9	1	5	1	3	0	1
0	0	1	0	2	2	10	2	6	0	2	2	3
0	0	1	1	3	3	11	3	7	1	3	2	3
0	1	0	0	4	4	12	0	4	4	6	4	5
0	1	0	1	5	5	13	1	5	5	7	4	5
0	1	1	0	6	6	14	2	6	4	6	6	7
0	1	1	1	7	7	15	3	7	5	7	6	7
1	0	0	0	8	0	8	8	12	8	10	8	9
1	0	0	1	9	1	9	9	13	9	11	8	9
1	0	1	0	10	2	10	10	14	8	10	10	11
1	0	1	1	11	3	11	11	15	9	11	10	11
1	1	0	0	12	4	12	8	12	12	14	12	13
1	1	0	1	13	5	13	9	13	13	15	12	13
1	1	1	0	14	6	14	10	14	12	14	14	15
1	1	1	1	15	7	15	11	15	13	15	14	15

1. Using functional complete tolerant (FCT) elements

One of the leading experts in the field of PLD FPGA development Yervant Zorian states: "Now the main problem of system on a chip repair is development of embedded technologies and methods of the logic repair that occupies no more than 10% of chip area" [12].

It is most important with Radiation Hardened By Design (RHBD) in military and aerospace applications [13].

The concept of the elements with redundant bases is suggested. This is functionally complete tolerant elements [14] (FCT-elements) those retain functional completeness in the terms of Post's lattice [15] under specific fault model (as example, under standard model [8, 9]. This allows the FPGA logic restoration after the faults. The CMOS functionally complete the tolerant element FCT-function (1) is depicted to Fig.2:

$$(\bar{x}_1 \vee \bar{x}_2)(\bar{x}_3 \vee \bar{x}_4) \quad (1)$$

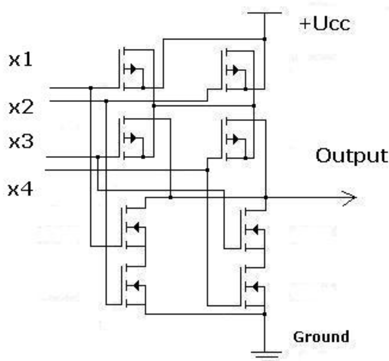


Fig. 2. The CMOS functionally complete tolerant element (FCTE) – function (1)

In the case of single constant failures lines or transistors functional completeness remains:

$$\begin{aligned}
&x_1^1 \Rightarrow \bar{x}_2(\bar{x}_3 \vee \bar{x}_4) = \overline{x_2 \vee x_3 x_4};\\
&x_2^1 \Rightarrow \bar{x}_1(\bar{x}_3 \vee \bar{x}_4) = \overline{x_1 \vee x_3 x_4};\\
&x_3^1 \Rightarrow (\bar{x}_1 \vee \bar{x}_2)\bar{x}_4 = \overline{x_1 x_2 \vee x_4};\\
&x_4^1 \Rightarrow (\bar{x}_1 \vee \bar{x}_2)\bar{x}_3 = \overline{x_1 x_2 \vee x_3};\\
&x_1^0 \Rightarrow (\bar{x}_3 \vee \bar{x}_4) = \overline{x_3 x_4};\; x_2^0 \Rightarrow (\bar{x}_3 \vee \bar{x}_4) = \overline{x_3 x_4};\\
&x_3^0 \Rightarrow (\bar{x}_1 \vee \bar{x}_2) = \overline{x_1 x_2};\; x_4^0 \Rightarrow (\bar{x}_1 \vee \bar{x}_2) = \overline{x_1 x_2}.
\end{aligned} \quad (2)$$

The dual version of FCT function is

$$\bar{x}_1 \bar{x}_2 \vee \bar{x}_3 \bar{x}_4 . \quad (3)$$

Use of FCTE as the element NOT makes possible to ensure failure resistance with the failures of any one transistor in the circuit of connection "+" and "Ground"- (Fig. 3). Exponential reliability function of the NOT FCTE (Fig.3) is described by (4):

$$P(t)_1 = [e^{-4 \cdot \lambda_T \cdot t} + 4 \cdot e^{-3 \cdot \lambda_T \cdot t}(1 - e^{-\lambda_T \cdot t})]^2 , \quad (4)$$

where λ_T is a transistor's failure rate.

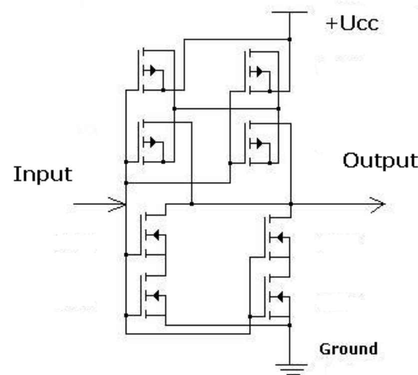


Fig. 3. The CMOS FCTE representation of the NOT function $(\bar{x} \vee \bar{x})(\bar{x} \vee \bar{x})$, Input = x

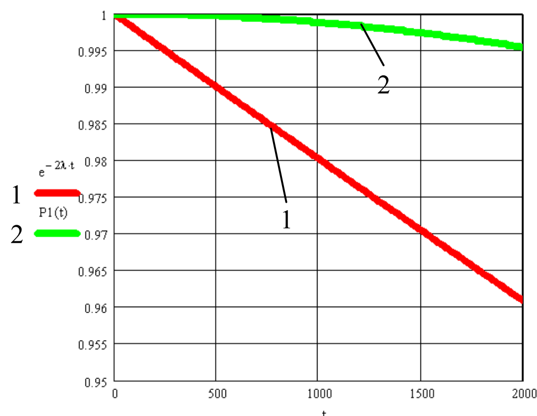


Fig. 4. Comparison of the exponential reliability functions of the NOT FCTE and simple NOT element (two transistors) $\lambda_T = 10^{-5}$

2. LUT+ FCTE FPGA

The proposed the logic element, which ensures the functionality at least of half LUT with the failure of any one transistor is presented on Fig.5.

Inverters in terms of the variables A, B, C, D can be built similarly, if it is required. Known LUTn without accounting the commutations of input variables is evaluated as follows.

A quantity of transistors in the tree of the transmitting transistors on n of variables is evaluated by (5):

$$L_{trLUTn} = 2^{n+1} - 2. \quad (5)$$

Taking into account inverters on the entrances of variable (2n), output inverters (in each of 2 transistors) we will obtain in all in the tree:

$$L_{trLUTn} = 2^{n+1} - 2 + 2 \cdot n + 2 = 2^{n+1} + 2 \cdot n. \quad (6)$$

Then reliability functions P0 (LUT) and P1 (LUT+ FCTE) are described (Fig.6) by expressions (7) – (8):

$$P(t)_1 = (e^{-(2^{n+1}+2n) \cdot \lambda_T \cdot t} + (2^{n+1}+2n) \times \\ \times e^{-(2^{n+1}+2n-1) \cdot \lambda_T \cdot t}(1-e^{-\lambda_T \cdot t})) \cdot [e^{-4 \cdot \lambda_T \cdot t} + \\ +4 \cdot e^{-3 \cdot \lambda_T \cdot t}(1-e^{-\lambda_T \cdot t})]^2. \quad (7)$$

$$P(t)_0 = [e^{-(2^{n+1}+2n) \cdot \lambda_T \cdot t} + (2^{n+1}+2n) \times \\ \times e^{-(2^{n+1}+2n-1) \cdot \lambda_T \cdot t}(1-e^{-\lambda_T \cdot t})] \cdot e^{-2 \cdot \lambda_T \cdot t}. \quad (8)$$

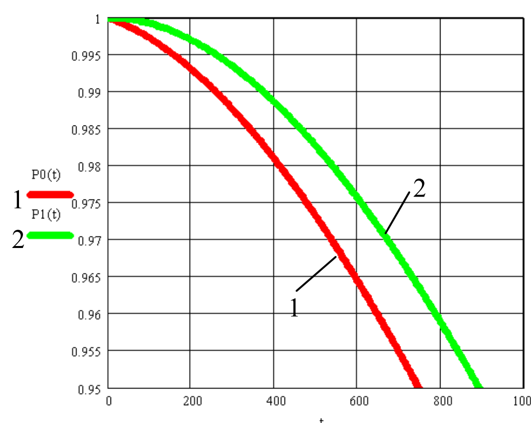


Fig. 6. Comparison of the exponential reliability functions of the LUT FCTE (P1) and LUT (P0) in MathCAD, $\lambda_T = 10^{-5}$

However, even LUT FCTE does not make possible it to be sultry SEU (Single Event Upset), furthermore, after fault functional possibilities LUT decrease two.

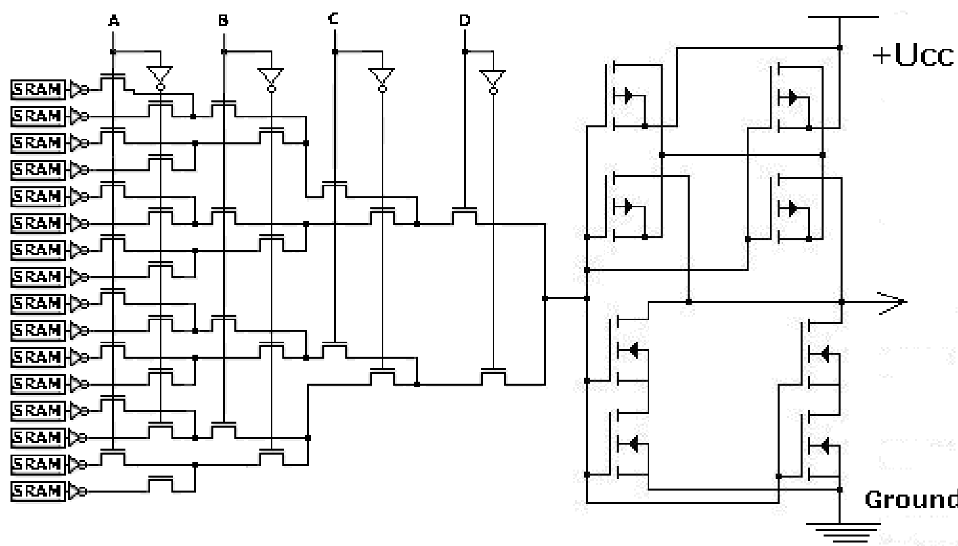


Fig. 5. Fault-tolerant LUT FPGA - LUT+ FCTE

3. Estimation of the triplexed tree of the transmitting transistors tree

The traditional method of guaranteeing the reliability is Triple Modular Redundancy (TMR). TMR uses three trees LUT with the majority element (or voting element), which realizes the following majority function (9):

$$z = k_1k_2 \vee k_2k_3 \vee k_1k_3 . \quad (9)$$

The expression of majority function in the basis of 2NAND takes the form:

$$\begin{aligned} z &= \overline{\overline{k_1k_2 \vee k_2k_3 \vee k_1k_3}} = \\ &= \overline{\overline{k_1k_2}\,\overline{k_2k_3}\,\overline{k_1k_3}} = \\ &= \overline{\overline{\overline{\overline{k_1k_2}\,\overline{k_2k_3}}}\,\overline{k_1k_3}}. \end{aligned} \quad (10)$$

The six elements of 2NAND are required, on each of 4 transistors, in total 24 transistors, delay 4τ, where τ is the delay of one element of 2NAND. We obtain (11):

$$L_{3trLUTn} = 3 \cdot (2^{n+1} + 2 \cdot n) + 24, n \geq 2 . \quad (11)$$

Thus, for n =4 we have 120+24=144 (transistor).

In the case of tripling of the majority element, the 72 transistors are needed (12):

$$L_{3tr3mLUTn} = 3 \cdot (2^{n+1} + 2 \cdot n) + 72 . \quad (12)$$

Thus, for n = 4 we have 120+72=192 (transistor).

4. Redundancy of the transmitting transistors

Similarly to the previous case, for FCTE lets carry out the redundancy of transmitting transistors (Fig.7) and (Fig. 8).

$$f_{1.1} = (x_i \vee x_i)(x_i \vee x_i) , \quad (13)$$

$$f_{1.2} = x_i x_i \vee x_i x_i . \quad (14)$$

$$f_{2.1} = (x_i \vee x_i \vee x_i)(x_i \vee x_i \vee x_i)(x_i \vee x_i \vee x_i) , \quad (15)$$

$$f_{2.2} = x_i x_i x_i \vee x_i x_i x_i \vee x_i x_i x_i . \quad (16)$$

For countering the failures in two transistors, the structures presented on Fig. 9 and Fig. 10 can be used.

For countering of three failures, it is necessary to use the following functions:

$$\begin{aligned} f_{3.1} = &(x_i \vee x_i \vee x_i \vee x_i)(x_i \vee x_i \vee x_i \vee x_i) \\ &(x_i \vee x_i \vee x_i \vee x_i)(x_i \vee x_i \vee x_i \vee x_i), \end{aligned} \quad (17)$$

$$f_{3.2} = x_i x_i x_i x_i \vee x_i x_i x_i x_i \vee x_i x_i x_i x_i \vee x_i x_i x_i x_i . \quad (18)$$

Thus using (13), (14) and by duplicating the entrances we obtain the complexity (19):

$$L_{4trLUTn} = 4 \cdot (2^{n+1} - 2) + 4 \cdot n + 8 . \quad (19)$$

Thus, for n =4 we have 120+16+8=144 (transistors).

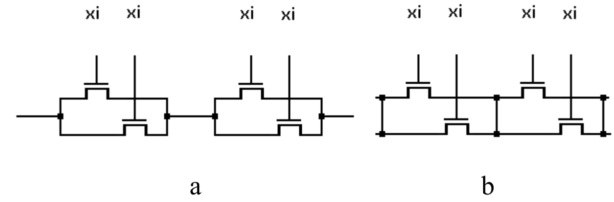


Fig. 7. Quadrupling of the transmitting transistors according to the versions of the function (13):
a – with one point of connection;
b – with two points of the connection

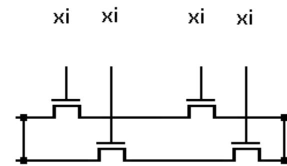


Fig. 8. Quadrupling of the transmitting transistors according to the versions of the function (14)

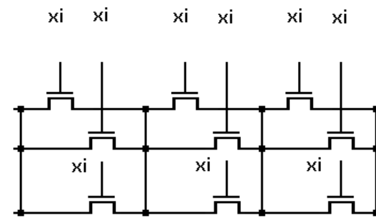


Fig. 9. Redundancy of the transmitting transistors according to the function (15)

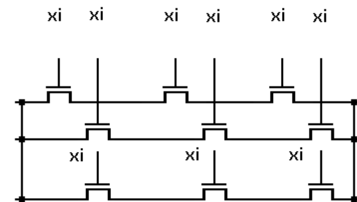


Fig. 10. Redundancy of the transmitting transistors according to the function (16)

4. Comparison of the exponential reliability functions of the Quadrupling LUT and the tripling LUT

Taking into account (11) the reliability function of the tripling LUT is described by the following expression (20):

$$P1(t) = (3 \cdot e^{-2\cdot(2^{n+1}+2n)\cdot\lambda\cdot t} - 2 \cdot e^{-3\cdot(2^{n+1}+2n)\cdot\lambda\cdot t}) \cdot e^{-24\cdot\lambda\cdot t}. \quad (20)$$

In the case of tripling of the majority element we obtain:

$$P1(t) = (3 \cdot e^{-2\cdot(2^{n+1}+2n)\cdot\lambda\cdot t} - 2 \cdot e^{-3\cdot(2^{n+1}+2n)\cdot\lambda\cdot t}) \times (3 \cdot e^{-2\cdot 24\cdot\lambda\cdot t} - 2 \cdot e^{-3\cdot 24\cdot\lambda\cdot t}. \quad (21)$$

The exponential reliability function of the Quadrupling LUT (QLUT) is described by expression (22):

$$P3(t) = [e^{-4\lambda t} + 4 \cdot e^{-3\lambda t}(1 - e^{-\lambda t})]^{(2^{n+1}-2)} \times [e^{-4\lambda t} + 4 \cdot e^{-3\lambda t}(1 - e^{-\lambda t})]^2 \times [e^{-2\lambda t} + 2 \cdot e^{-\lambda t}(1 - e^{-\lambda t})]^n. \quad (22)$$

Comparison of the exponential reliability functions of the QLUT (P3) and the tripling LUT (P2,P1) are represented on Figure 11.

Thus, the version of redundancy P3 according to the function $f_{1.2} = x_i x_i \vee x_i x_i$ considerably more preferable than reliability functions of the version P2 and all the more P1. Comparison of the complexity in a quantity of the transistors of the tripling LUT (Expression12-L3) and QLUT-L4 is represented on Fig. 12

Thus, to n=6 the version of redundancy according to the function $f_{1.2} = x_i x_i \vee x_i x_i$ is preferable based on the reliability function and the complexity.

5. Comparison of the versions of fault tolerant LUT taking into account the redundancy SRAM cell

We will consider the complexity SRAM cell of -6 transistors. Let us estimate version TMR (Triple Modular Redundancy).

In this case, SRAM cell is included in each of three TMR channels and complexity LUT it takes the form:

$$L_{LUT_n+(SRAM+NOT)} = 2^{n+1} - 2 + 2 \cdot n + 2 + (6+2) \cdot 2^n = 10 \cdot 2^n + 2 \cdot n. \quad (23)$$

Taking into account (23) the reliability functions of the tripling LUT + SRAM cell is described by expression (24):

$$Ptt(1) = (3 \cdot e^{-2\cdot(10\cdot 2^n+2n)\cdot\lambda t} - 2 \cdot e^{-3\cdot(10\cdot 2^n+2n)\cdot\lambda\cdot t}) \cdot e^{-24\cdot\lambda\cdot t}. \quad (24)$$

In the case of tripling of the majority element (25):

$$Ptt3(t) = (3 \cdot e^{-2(10\cdot 2^n+2n)\cdot\lambda\cdot t} - 2 \cdot e^{-3(10\cdot 2^n+2n)\cdot\lambda t}) \times (3 \cdot e^{-2\cdot 24\cdot\lambda\cdot t} - 2 \cdot e^{-3\cdot 24\cdot\lambda\cdot t}). \quad (25)$$

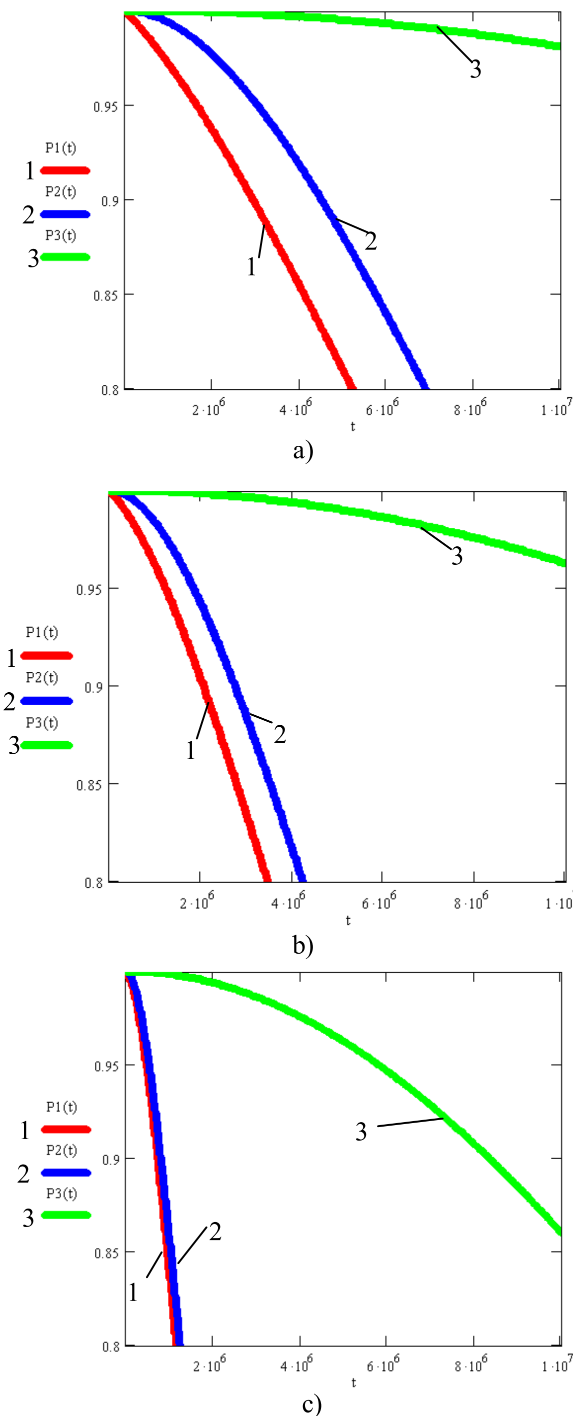


Fig. 11. Comparison of the exponential reliability functions of the Quadrupling LUT (P3) and the tripling LUT (P2,P1) MathCAD, a) n=4, b) n=5, c) n=6, $\lambda = 10^{-9}$

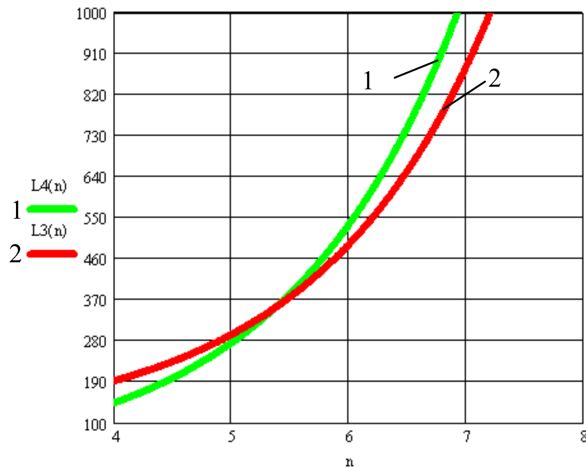


Fig. 12. Comparison of the complexity in a quantity of the transistors of the tripling LUT-L3 and QLUT-L4

The reliability functions of the QLUT+ SRAM cell is described by the following expression:

$$\begin{aligned} Pfct(t) = {} & [e^{-4\lambda t} + 4 \cdot e^{-3\lambda t}(1-e^{-\lambda t})]^{6 \cdot 2^n} \times \\ & \times [e^{-4\lambda t} + 4 \cdot e^{-3\lambda t}(1-e^{-\lambda t})]^{(2^{n+1}-2)} \times \\ & \times [e^{-4\lambda t} + 4 \cdot e^{-3\lambda t}(1-e^{-\lambda t})]^2 \times \\ & \times [e^{-2\lambda t} + 2 \cdot e^{-\lambda t}(1-e^{-\lambda t})]^n . \end{aligned} \quad (26)$$

We obtain for unreserved LUT (27):

$$e^{-(10 \cdot 2^n + 2n) \cdot \lambda t}. \quad (27)$$

The comparison of all enumerated versions (24)-(27) is represented on Fig. 13.

Version (Pfct) undoubtedly has a complexity approximately to 30% greater than Ptt3 (Fig. 14). But this is relatively “cheap”!

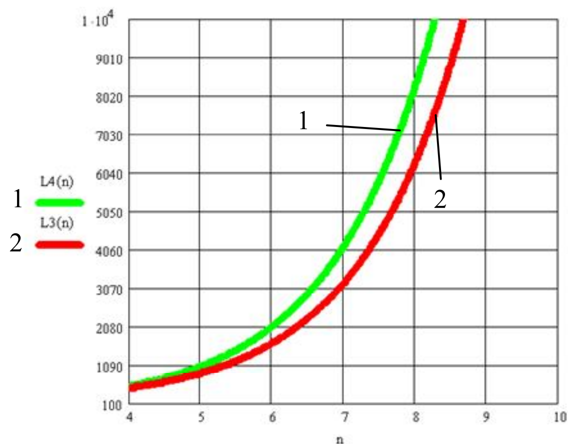
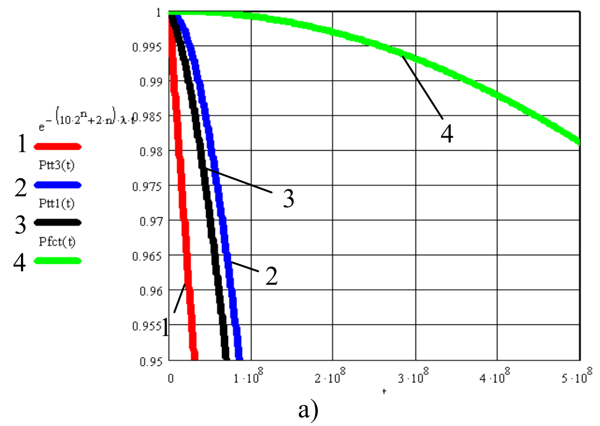
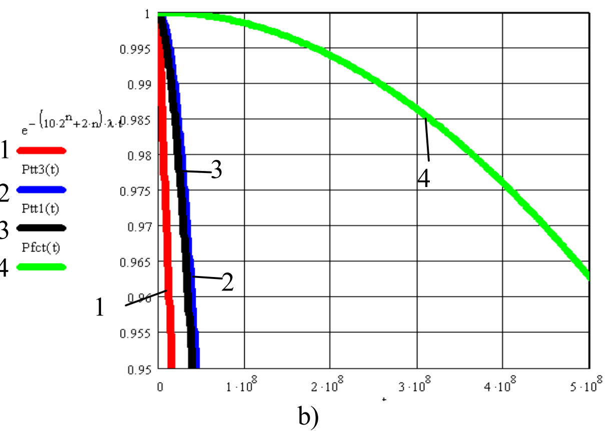
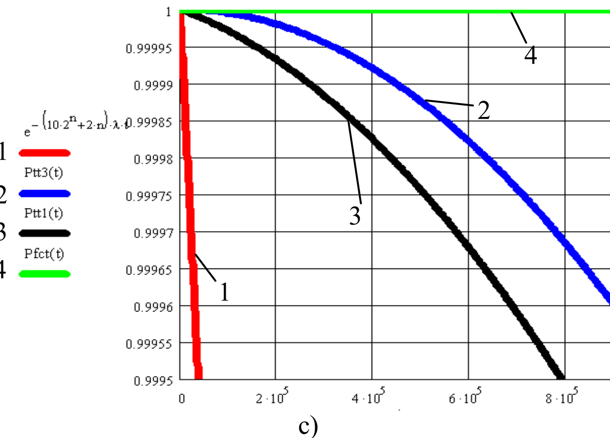


Fig. 14. Comparison of the complexity in a quantity of the transistors of the QLUT+ SRAM cell (L4) and the tripling L3







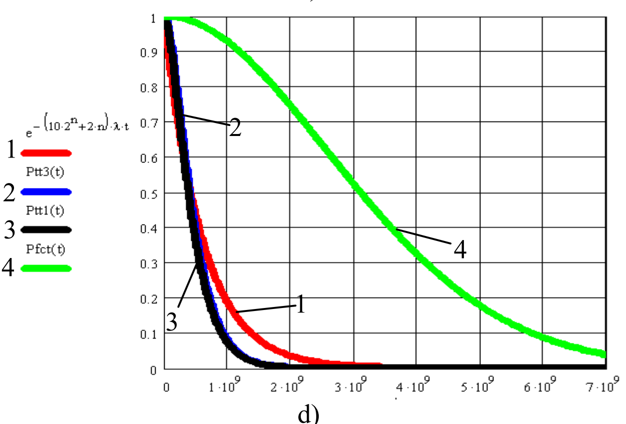


Fig. 13. Comparison of the exponential reliability functions of the QLUT+ SRAM cell (Pfct), (Ptt1,Ptt3) and the unreserved LUT in MathCAD, $\lambda=10^{-11}$, n = a) 4; b) 5; c) 7; d) 4

Conclusion

The redundancy LUT FPGA according to the function $x_i x_i \vee x_i x_i$ appears to be more preferable on the reliability function, than tripling, moreover expenditure for this - order 30%, that not too it is much in comparison with a multiple increase in the equipment during the introduction of additional channels.

Furthermore, is reached the gain of more than 70% of maximally possible exponential reliability function in comparison with the tripling in case of tripling of the majority element (Fig. 13.d).

If we reserve only the tree of transistors, then to n=6 the version of redundancy according to the function $x_i x_i \vee x_i x_i$ is preferable both on the reliability function and in the complexity.

References

1. *Betz, V. How much logic should goin an fpga logic block? [Text] / V. Betz, J. Rose// IEEE Design and Test Magazine. Spring. – 1998.*
2. *Betz, V. FPGA routing architecture: segmentation and buffering to optimize speed and density [Text] / V. Betz, J. Rose// IEEE Design and Test Magazine, Lewis D. et al., Proc. FPGA-02.–Spring, 1999.*
3. *Ahmed, E. The effect of lut and cluster size on deep-submicron FPGA performance and density [Text]/ E. Ahmed, J. Rose // Proc FPGA-00.*
4. *Czajkowski, T. S. A Synthesis oriented omniscient manual editor [Text] / T. S. Czajkowski, J. Rose // FPGA'04. Monterey, California, USA, 22- 24 Feb. 2004.*
5. *FLEX 10K. Embedded programmable logic device family. March 2001, Ver. 4.1 [Electronic resource].– Available to: http://www.altera.com.*
6. *Stratix III. Device handbook. July. 2009. Vol. 1. – Software version 9.0 [Electronic resource]. – Available to:http:// www.altera.com.*
7. *FPGA & SoC product [Electronic resource]. – Available to: http://microsemi.com/products/fpga-soc/fpga-and-soc/.*
8. *Stuck-at fault [Electronic resource]. – Available to: http://en.wikipedia.org/wiki/Stuck-at_fault.*
9. *Bridging fault [Electronic resource]. – Available to: http://en.wikipedia.org/wiki/ Bridging_fault.*
10. *Tyurin, S. F. The principle of recovery logic FPGA for critical applications by adapting to failures of logic elements [Text] / S. F. Tyurin, A. V. Grekov, O. A. Gromov // World Applied Sciences Journal. – 2013. – Vol. 26, № 3. – P. 328 – 332.*
11. *Tyurin, S. F. A residual basis search algorithm of fault-tolerant programmable logic integrated circuits [Text] / S. F. Tyurin, O. A. Gromov // Russian Electrical Engineering. – 2013. – Vol. 84, №11. – P. 647 - 651.*
12. *Yervant, Z. Gest editors' introduction: Design for yield and reliability [Text] / Z. Yervant, G. Dmytris // IEEE Design & Test of Computers. – May-June 2004. – P. 177-182.*
13. *Mayer, Donald C. Designing integrated circuits to withstand space radiation [Electronic resource]. – Available to: http://www.aero.org/publications/crosslink/ summer2003/06.*
14. *Tyurin, S. F. Retention of functional completeness of Boolean functions under "failures" of the arguments [Text] / S. F. Tyurin // Automation and Remote Control. – 1999. – Vol. 60, № 9.2. – P. 1360 – 1367.*
15. *Post, E. L. The two-valued iterative systems of mathematical logic [Text] / E. L. Post // Annals of Mathematics studies, Vol. 5, Princeton University Press, Princeton, 1941. – P. 122.*

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ОТКАЗОУСТОЙЧИВЫЙ ЛОГИЧЕСКИЙ ЭЛЕМЕНТ ПЛИС FPGA

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Описывается отказоустойчивый логический элемент ПЛИС FPGA (field-programmable gate array), показывается, что при четырёх – пяти переменных резервирование путём учетверения транзисторов дерева LUT (Look Up Table) предпочтительней, чем троирование, не только по вероятности безотказной работы, но и по сложности. Относительно конфигурационной памяти SRAM такое резервирование также целесообразней троирования даже с тремя мажоритарами. В случае резервирования LUT вместе с конфигурационной памятью SRAM можно получить значительный выигрыш в вероятности безотказной работы порядка 70% относительно максимально возможного за относительно умеренные затраты порядка 30%, что является также приемлемым, сравнительно с многократным увеличением объема используемого оборудования, при введении дополнительного канала.

Ключевые слова: отказоустойчивый логический элемент ПЛИС FPGA - LUT – Look Up Table, интенсивность отказов, вероятность безотказной работы, резервирование, элемент с избыточным базисом – функционально-полный толерантный (ФПТ) элемент, конфигурационная память SRAM.

ВІДМОВОСТІЙКІ ЛОГІЧНІ ЕЛЕМЕНТ ПЛІС FPGA

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У статті пропонується відмовостійкі логічні елемент FPGA (field-programmable gate array) для критичних застосувань. Показується, що при чотирьох - п'яти змінних резервування шляхом почетвереній транзисторів дерева LUT (Look Up Table) краще, ніж троірованіе, не тільки по ймовірності безвідмовної роботи, але і по складності. Щодо конфігураційної пам'яті SRAM таке резервування також доцільніше троірованія навіть з трьома мажоритарії. У разі резервування LUT разом з конфігураційною пам'яттю SRAM можна отримати значний виграш у ймовірності безвідмовної роботи близько 70% щодо максимально можливого за відносно помірні витрати близько 30%, що є прийнятним, порівняно з багаторазовим збільшенням обсягу використовуваного обладнання, при введенні нового каналу.

Ключові слова: адаптація, відмови, програмована користувачем вентильна матриця, таблиця пошуку, логічний елемент, відмовостійкість.

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