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SYNTESIS AND ANALYSIS OF SELF-TIMED FUNCTIONALLY COMPLETE TOLERANT ELEMENT

The paper proposes a complete self-timed functional tolerance element - ST FCT. It's described results of the functional simulation, verification of semi-modular, as well as an example of the synthesis of self-timed circuits in CAD MultiSim and comparison of performance at different supply voltages. Application of the proposed element allows the synthesis of self-timed circuits in a redundant fault-tolerant basis preserving functional completeness in terms of failures, enables the automatic synthesis of custom self-timed combinational circuits, which could remain operational state at reduced voltage.

***Key words**: self-timed circuits, reduced supply voltage, functionally complete tolerance element, CAD, semi-modular.*

Introduction

Modern digital electronics faced again with the problem of reduce energy consumption when saving performance. It is impossible indefinitely increase the battery capacity for high-power processors, such as smart phones. One solution is to implement self-timed approach that can significantly reduce the energy consumption with a similar, and sometimes, with better performance.

Created by Handshake Solutions self-timed core when saving performance provides 3 times less energy. Company Achronix also developed a self-timed FPGA-chip, clocked at up to 1.5 GHz and superior in performance of existing FPGA from Altera and Xilinix [1]. The developed technique self-timed pipelined scheme [2], due to its redundancy, is not suitable for creating arbitrary combination schemes. Basis of self-timed circuits in need of development, and there is no method of automated synthesis of self-timed circuits.

In this study will be presented with a new basic item self-timed circuits - strictly self-timed functional complete tolerance element.

1. Synthesis of functional circuit

Let us divide a self-timed functionally complete tolerant element to the functional blocks (fig. 1, table 1):

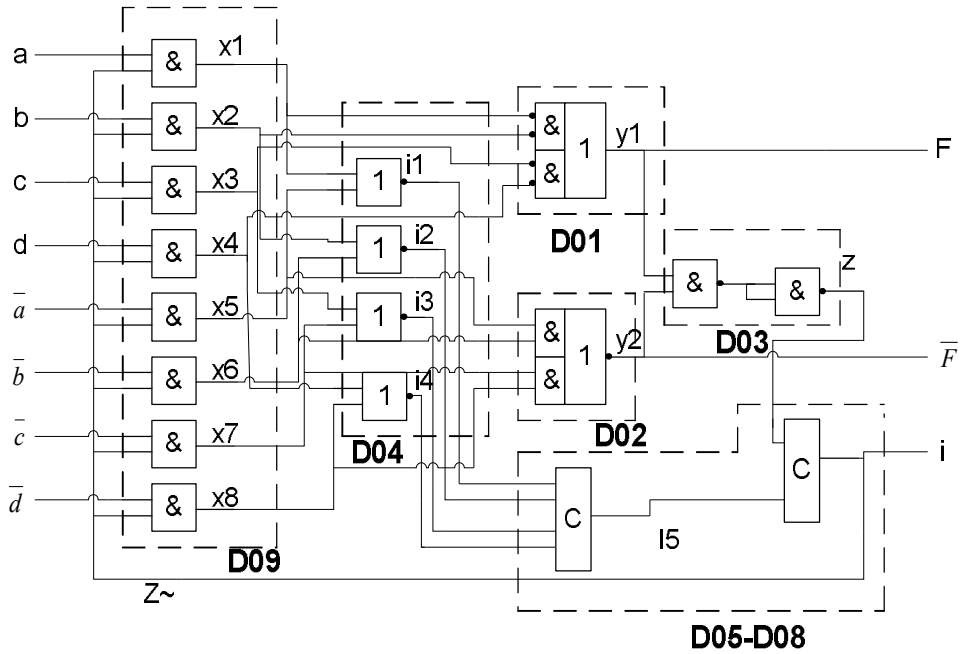

Fig. 1. Functional scheme of the ST FCT element

Table 1

Truth table of ST FCT element

S	abcd	F	$\overline{F}$	I
0	----	1	1	1
1	0000	1	0	0
1	0001	1	0	0
1	0010	1	0	0
1	0011	1	0	0
1	0100	1	0	0
1	0101	0	1	0
1	0110	0	1	0
1	0111	0	1	0
1	1000	1	0	0
1	1001	0	1	0
1	1010	0	1	0
1	1011	0	1	0
1	1100	1	0	0
1	1101	0	1	0
1	1110	0	1	0
1	1111	0	1	0

1. Main channel – consist from FCT-element, provides the function $f = \overline{x_1 x_2} \vee \overline{x_3 x_4}$.

2. Additional channel – consist from FCT2-element, $f = \overline{x_1 x_2 \vee x_3 x_4}$.

3. Indicator: captures the state NULL output.

4. Input indicator: captures NULL state at the input.

5. C-elements, they combine outputs of indicators to form a common signal.

6. Spacer block: sets element in state NULL.

2. Synthesis of schematic electrical diagram

The first block is shown on fig. 2, the main data path, a FCT-element

$$f = \overline{x_1 x_2} \vee \overline{x_3 x_4} .$$

It is implemented with 8 CMOS transistors, four of each type. 1,2,3,4 - inputs of element, 5 - Power Bus, 6 – zero bus, 7 - output [3].

The second block is shown on fig. 3, the additional data channel, inverse FCT element

$$f = \overline{x_1 x_2 \vee x_3 x_4} .$$

As well as the D01 sold eight CMOS transistors, four of each type. 1,2,3,4 - inputs, 5 - Power Bus, 6 - bus zero, 7 - exit. Here, the first line of transistors performs the conjunction of inputs, the second line – 2NOR-gate.

The third block is shown on fig. 4, the indicator combines output nodes D01, D02. The block implements the function $I = \overline{f_1 \wedge f_2}$, and based on four CMOS transistors, two of each type. 1.2 - inputs of the element, 3 - Power Bus, 4,5 - bus zero, 6 - output.

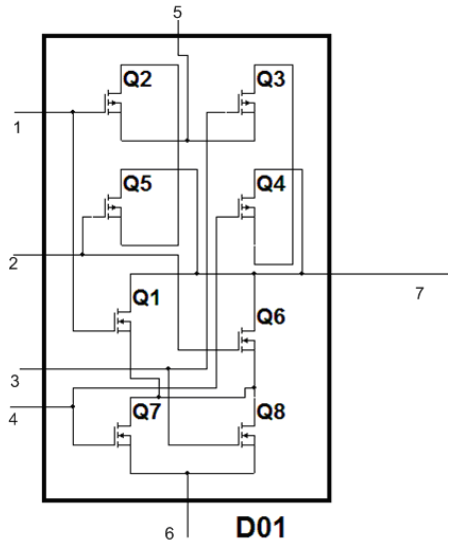

Fig. 2. Circuit diagram ofFCT-element

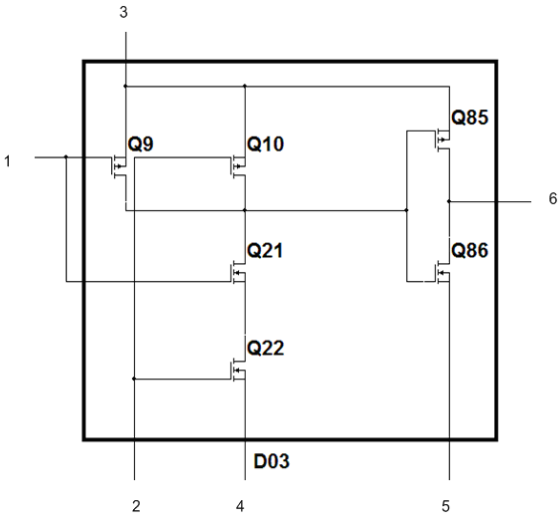

Fig. 3. Circuit diagram of FCT-2 element

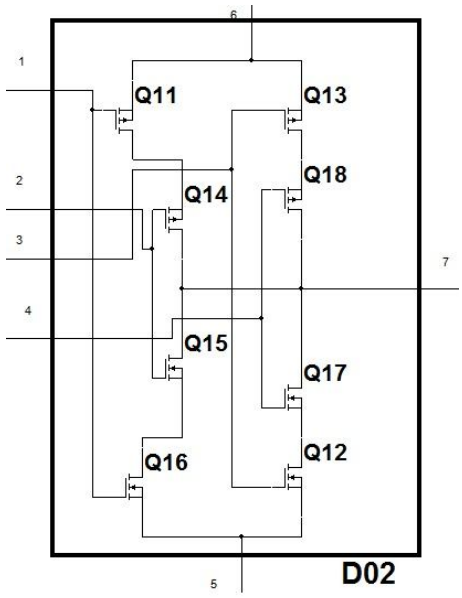

Fig. 4. Circuit diagram of indicator 2NAND

The fourth block is shown on fig. 5, indication unit of input variable, contains four 2NOR elements. Block specifies the end of NULL phase for each variable separately $I_n = \overline{x_n \vee x_{n+4}}$ $I = 1$ - NULL phase $I = 0$ - working phase.

1 - Bus zero. 5.9 - Power Bus.

2.6 - inputs, 14 output of the third element.

3.4 - input, 12 output of the first element.

7.11 - input, 13 output of the second element.

8.10 - inputs, 15 output of the fourth element.

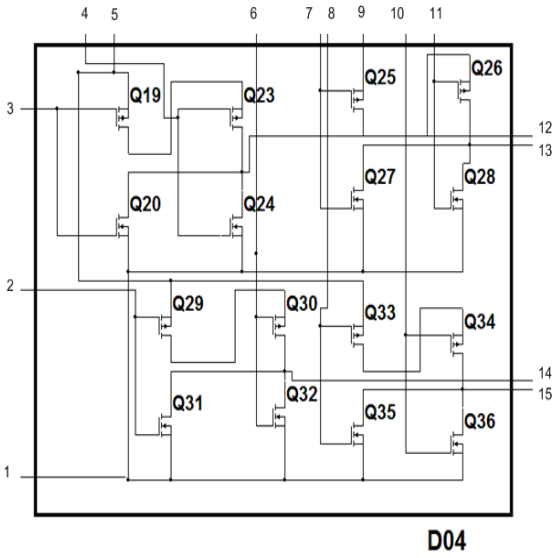

Fig. 5. Circuit diagram of indication unit of input variable

The fifth block, two G-flip-flops also called Mullers C-gate. Hysteresis triggers with two entrances and four. 1, 2 - inputs, 3 - output, 4-bus power supply, 5 - bus zero for the first. 1,2,3,4 – Inputs, 5 –bus power supply, 6 – bus zero, 7-output for second. The first element is formed a 12 CMOS transistors. The second element consist 24 CMOS transistors. The outputs of D04 are connected to the inputs of the D05. Outputs of D05 and D03 are connected to D06. The output of D06 is an indicator end of the transition process for the element (table 2, fig. 6, 7).

Table 2

Truth table of G-flip-flop

A	B	Y
0	0	0
0	1	Y_{n-1}
1	0	Y_{n-1}
1	1	1

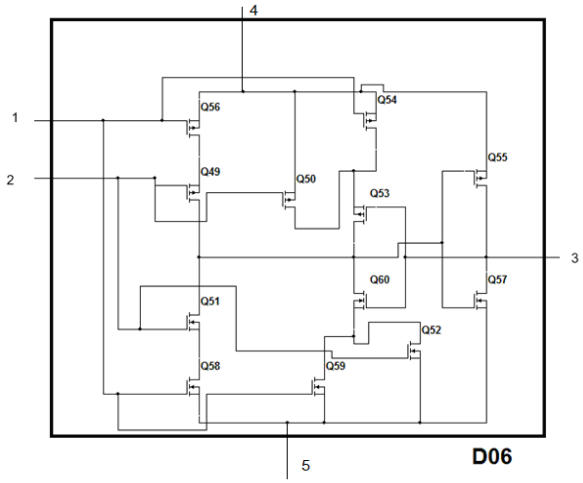

Fig. 6. Circuit diagram of G-flip-flop with two entrances

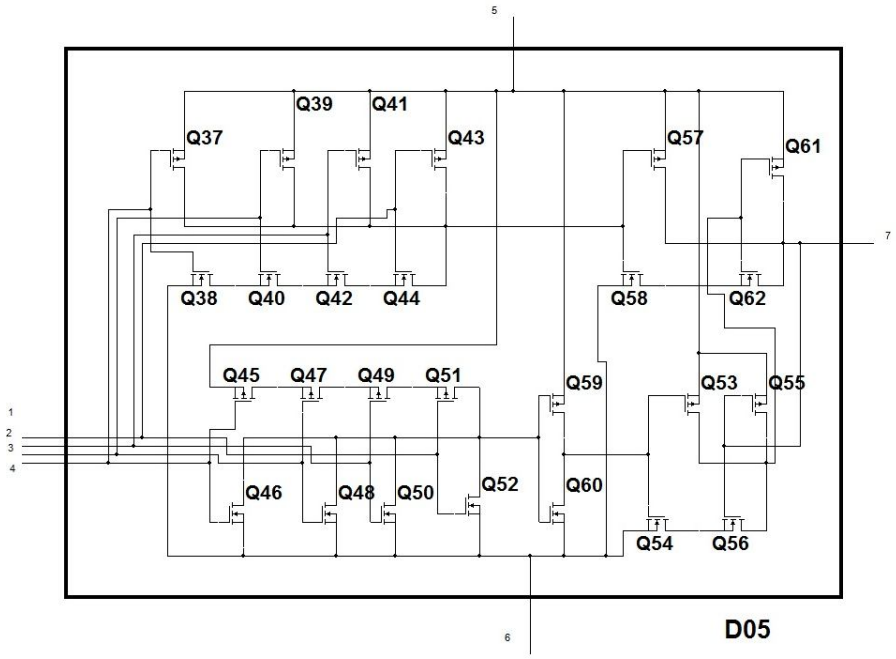

Fig. 7. Circuit diagram of G-flip-flop with four entrances

The fifth block, the block spacer consists of eight elements 2AND CMOS logic. The first input of each element is connected to a variable or inverse variable. The second input is connected to the signal request, or, for a self-timed mode, to output D08.

3. Analysis of the ST FCT element

Initially analyzed semi-modular property, it uses the subsystem Tranal, CAD Forcage. For the analysis of the scheme it must be represented as a model of Muller. For the initial state in the Muller model is chosen state NULL [4] (fig. 8).

After verification semi-modularity we can analyze the functional parameters. Functional properties will be analyzed in NI MultiSim. Transistors selected for implementation: P-channel enhancement mode vertical D-MOS transistor 0.25A, 60V, 7.5 W, N - Channel Mode increase vertical DMOS FET 0.2A, 60V, 5 ohms. Self-timed circuits have two delays: delay of getting DATA and delay of getting NULL. The sum of these delays gives us a complex delay circuit. It should be noted that the self-timed circuits has not the highest possible speed, in addition to the delay switching transistors it has delay of indicator unit. First, get a delay in normal conditions, with a supply voltage of 5V (fig. 9).

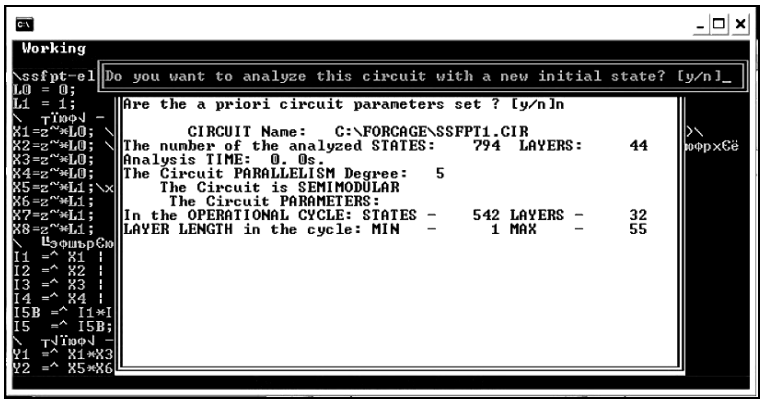

Fig. 8. Analysis of semi-modular

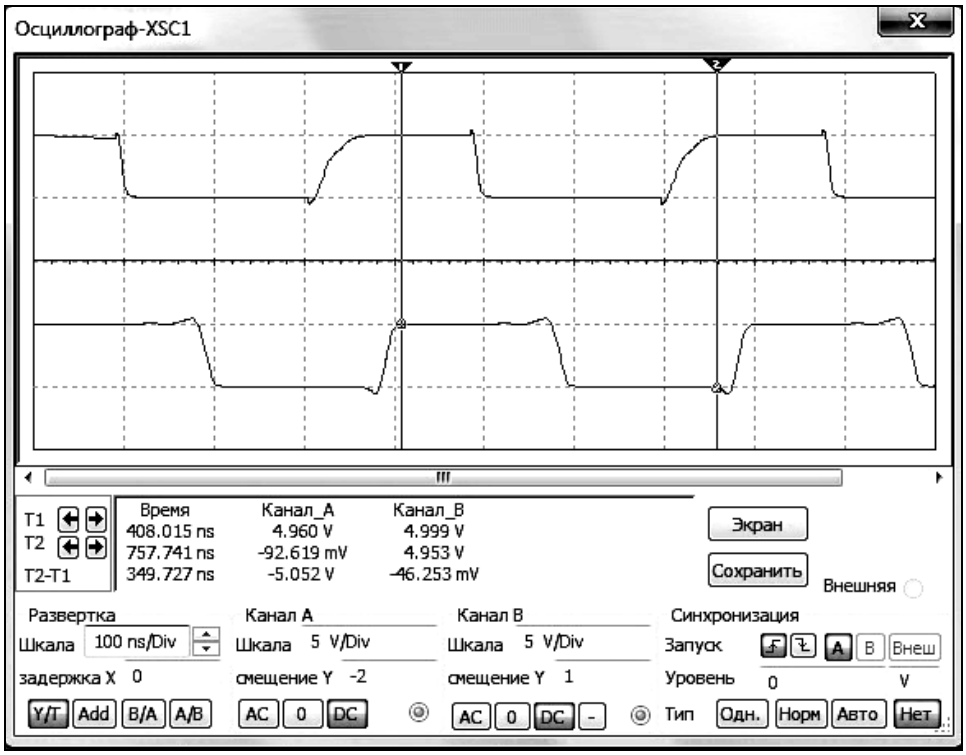

Fig. 9. Timing diagram element at a supply voltage of 5V

Then, test the functionality of the circuit when the voltage drops. If the voltage drops below 2.6 V transistors stop switch. The lower voltage threshold is set at 3B, which is 40% lower (fig. 10).

Timing diagrams are obtained with an oscilloscope. Upper pulse - output f2 (inverted channel), lower pulse - signal indicator. In self-timed mode, period of indicator is equal a delay of circuit. According to the

scope for this type of transistor, the time delay was 350 ns for 5V and 1.639 us at 3V. Thus, when supply voltage is reduced 40% the delay will be increased 4.7 times.

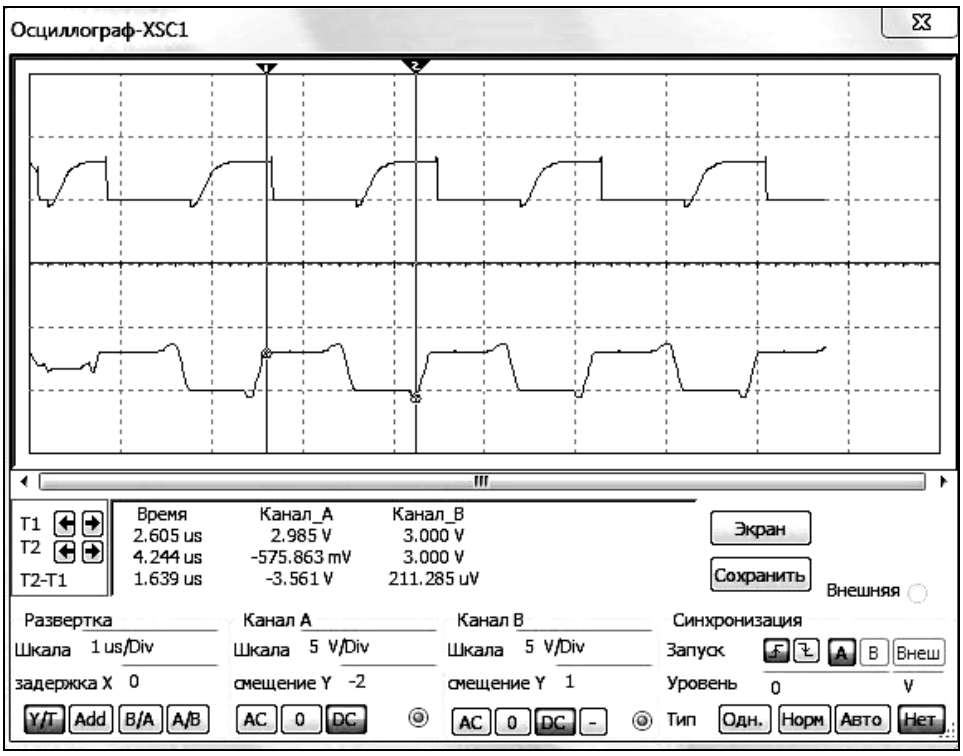

Fig. 10. Timing diagram element at a supply voltage of 3V

Now compare the complexity of ST XOR circuits realize by princip of conveyor scheme and our block. Calculation of complexity ST FCT-element:

- The main channel (FPT-element) - 8 CMOS transistors
- Additional channel (FPT2 element) - 8 CMOS transistors
- The output indicator (2NAND, with subsequent inversion) - 6 CMOS transistors
- The input indicator (4 items 2NOR) - 4 * 4 = 16 CMOS transistors
- Block spacer (8 items 2I) - 8 * 2 = 16 CMOS transistors
- 2 trigger hysteresis - 12 + 24 = 36 CMOS transistors

The total complexity of the scheme

22 +16 +16 +36 = 90 transistors.

Quite a lot, but the element contains all the necessary components to build self-timed circuits.

Consider the implementation of combinational functions FPT element on the princip of conveyor scheme, all units will also be built in CMOS transistors:

- Main Channel - 8 transistors
- Additional channel - 8 transistors
- Indicator - 2 transistors
- Register at the entrance - 8 G-Trigger, 8 * 12 = 96 transistors
- Register at the output - 2 G-flip-flops, 2 * 12 = 24 transistors

The final complexity of the scheme – 18+ 96+24 = 138 transistors. Conveyor schemes are not designed for a realization of combinational functions, as well as require a good knowledge of the engineer in the field of self-timed circuits.

The use of the SS FPT element as a basis, allows us to build combinational circuits using standard methods with only two differences:

1. Inverse variables must be connected;
2. Necessary to ensure the transmission of control signals.

The rest of the process of creating schemes will not be anything different.

Conclusion

Thus, it is proposed a basis to create self-timed circuits, which provide lower power consumption and better performance. This basis can win in difficulty of implementation, and also simplifies the process of design self-timed circuits, allowing to it automate. In the future we plan to adapt the algorithm of synthesis in FCT-basis for self-timed circuits. To ensure the best performance self-timed circuits, necessary to reduce the redundancy entered by unit of indicating and spacer.

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СИНТЕЗ І АНАЛІЗ СУВОРО САМОСІНХРОННОГО ФУНКЦІОНАЛЬНО-ПОВНОГО ТОЛЕРАНТНОГО ЕЛЕМЕНТУ

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У статті пропонується самосінхронний функціонально-повний толерантний елемент – СС ФПТ. Описано його функціональне моделювання, перевірка полумодулярності і порівняння продуктивності при різних напругах живлення, а також наведено приклад синтезу самосінхронної схеми в САПР MultiSim. Застосування запропонованого елемента дозволяє синтезувати самосінхронні відмовостійкі схеми в надмірному базисі, який зберігає функціональну повноту в умовах відмов, забезпечує можливість автоматичного синтезу нестандартних комбінаційних самосінхронних схем, що зберігають працездатність при зниженій напрузі живлення.

Ключові слова: самосінхронні схеми, знижена напруга живлення, функціонально-повний толерантний елемент, САПР, напівмодулярність.

СИНТЕЗ И АНАЛИЗ СТРОГО САМОСИНХРОННОГО ФУНКЦИОНАЛЬНО-ПОЛНОГО ТОЛЕРАНТНОГО ЭЛЕМЕНТА

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В статье предлагается самосинхронный функционально-полный толерантный элемент – СС ФПТ. Описано его функциональное моделирование, проводится проверка полумодулярности и сравнения быстродействия при различных напряжениях питания, а так же приведен пример синтеза самосинхронной схемы в САПР MultiSim. Применение предложенного элемента позволяет синтезировать самосинхронные отказоустойчивые схемы в избыточном базисе, сохраняющем функциональную полноту в условиях отказов, обеспечивает возможность автоматического синтеза нестандартных комбинационных самосинхронных схем, сохраняющих работоспособность при пониженном напряжении питания.

Ключевые слова: самосинхронные схемы, пониженное напряжение питания, функционально-полный толерантный элемент, САПР, полумодулярность.

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