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FPGA-BASED DIGITAL RECIRCULATOR

FPGA-based realization of a digital recirculator meant for the ensuring digital spread spectrum signals synchronization in the communication systems with code division multiple access in the small ratio signal/noise conditions after the compression in the programmable digital matched filter (PDMF) is presented in this paper. Synthesized VHDL-model is presented in the RTL-level and is implemented in the FPGA ALTERA CYCLONE II EP2C70F672C6 using CAD QUARTUS. The ways of logic elements quantity reduction in the FPGA are proposed.

Keywords: *code division, FPGA, recirculator, synchronization, and digital spread spectrum signals (DSSS).*

Introduction

In the communication systems with code division channels during using signals with base more then 1000 even after signals compression in the matched filter [1] the signal level in the output of the radio channel may be 26-30 dB less then the noise level. This may be enough for the given reception noise stability ensuring, but it is supposed additional energy reserve providing for the effective functioning of the synchronization channel by the clock frequency. Often for this purpose it is used the comb filters [2]. When digital matched filters are used, it is convenient to use digital recirculator [3] for the comb filters realization. They can be realized on the FPGA basis [4,5] from different vendors such as ALTERA [6] and XILINX [7], and are embedded in their crystals with hardware description languages VHDL, Verilog HDL, SystemC and others.

1. Recirculator

In the fig. 2 the module called "RECIRCULATOR" is presented on the RTL level. This module is implemented in the FPGA ALTERA CYCLONE II EP2C70F672C6 using CAD QUARTUS [6] development software.

This system consists of: DD1 – the block of input and stored in the recirculator values addition (CUR_PLUS_LAST); DD2 – the module of the digital recirculator address writing and reading control (ADDRESS); DD3 – dual-port random access memory (LPM_RAM_DP); DD4 – the block of multiplication by the feedback coefficient α (MULT_ALFA);

The equation that describes recirculator behavior has the form

$$R_i = Z + R_i \cdot \alpha , \qquad (1)$$

where

$$\alpha = \frac{2^n - 1}{2^n}, n \in Z . \qquad (2)$$

Feedback α coefficient values during variation power degree values are presented in the table 1.

Table 1

Feedback α coefficient values

n	0	1	2	3	4	5
$\alpha = \frac{2^n - 1}{2^n}$	0	$\frac{1}{2}$	$\frac{3}{4}$	$\frac{7}{8}$	$\frac{15}{16}$	$\frac{31}{32}$

Convolution value is following t o the input of recirculator which is realized using four modules: DD1-DD4 (Fig.2). On projecting with VHDL usage the recirculator may be presented in several ways: as separated, parameterized data type (massive) – type MEMORY is array (0 to 127) of signed(5*N+1 downto 0); or with library component usage of random access memory (lpm_ram_dp). After the VHDL-model synthesis in the second case, it is required considerably less quantity of FPGA logic elements (<1%) comparatively with the first case (≈40%) in the equal digit capacity. As it is known, altdpram does not support FPGA Cyclone II device family. Instead, CAD QUARTUS attempts to make a best-case memory conversions, but power-up states and read during write behavior are different for Cyclone II devices.

The address of values reading and writing in the recirculator is formed inside block DD2. On the falling edge of CLK_m signal the reading address from RAM is formed and on the rising edge the data stored in the RAM is read, multiplied by α coefficient and is add with coming in the recirculator input value. On the falling edge of the next clock impulse the result is written by the same address. For the data writing, in the address equal previous, in the two-step consecutive order, the writing address is formed by the block DD1, two clocks earlier comparatively with reading address. Therefore,

the writing address is passing ahead by two clocks and reading address is delayed, as in the figure 1 is shown.

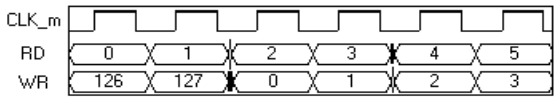

Fig. 1. Signal time graphs of the DD2 module

In the input POW of the DD4 module, the power value is inputted. It is used during feedback coefficient calculation, according to the formula (2), by which the values from recirculator output are followed. As it is well known during projecting with VHDL usage the synthesis of real data type is not supported in the CAD QUARTUS.

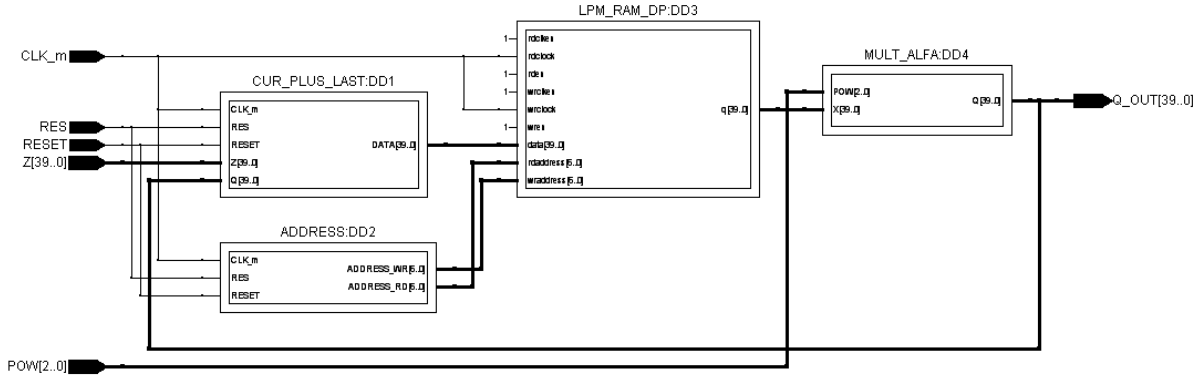

Fig. 2. Schema of a digital recirculator in the RTL-level

So for the values multiplication, followed from the output of recirculator by the coefficient α that is less then unity, it is supposed to use shift operators for the multiplication and division by the value multiple of two. Thus, multiplying by the numerator of coefficient α we perform left logical shift of multiplicand POW times and realize the difference of obtained value and the result of multiplication by unity in the numerator. The result is divided by the denominator with right logical shift POW times.

In the result, the coefficient α multiplication VHDL program has the form: Q<=SHR((SHL(X,POW)-X),X); where x – the value in the output of recirculator. After the synthesis of such a VHDL code the obtained schema found combinational. The schema in the RTL-level is presented in the figure 3.

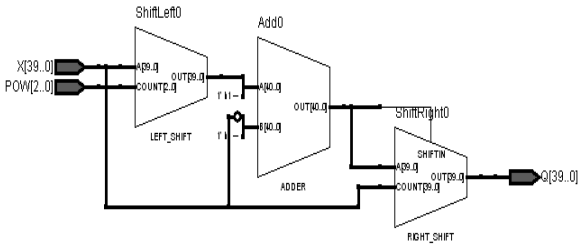

Fig. 3. Feedback α multiplication schema in the RTL-level

In the module DD1, the multiplied by the feedback coefficient α values are stored in the recirculator and are add with followed values in the in put of a recirculator. The schema in the RTL-level of this module is presented in the figure 4. Logical equation of the shema presented above has the form:

$$\mathrm{DATA} = (\mathrm{Z}+\mathrm{Q}) \wedge \overline{\mathrm{CLK\_m}} \wedge \left(\overline{\mathrm{RESET}} \vee \overline{\mathrm{RES}}\right) \quad (3)$$

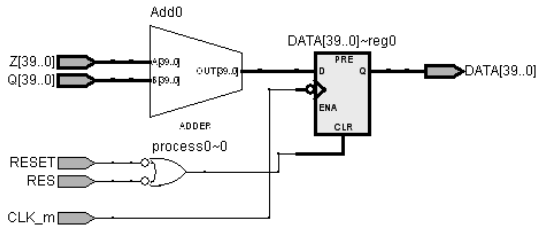

Fig. 4. The schema of DD1 module in the RTL-level

During digital recirculator functioning in the consistence of the synchronizing system all modules DD1-DD4 clocking is performed by the falling edge of the clock impulse CLK_m. From the beginning all cells of the RAM are equal to zero. In the figure 5 the signal time graphs are presented to illustrate behavior of the digital recirculator when the only one value equal to one is followed to its input Z. As we can see in the figure 5 each 128 interval clocks the stored in the recirculator value is increasing by 1, thus it accumulates the input influences in itself. When the feedback α is equal to zero the recirculator may occure in the overflow state. It is determined and remembered the address of jth subinterval where the observed process maximum value is situated. If to suppose that the signal convolution element is found in the jth subinterval, then with probabilities q exactly in this subinterval will be found the observed process maximum value. For the given trustworthiness providing of the sound decision about subinterval address, where the element convolution is presented, the procedure is repeated as long as the address of jth subinterval is repeated m times (or any others subinterval). For all that the probability of the false synchronization is equal to

$$P_{лс} = \left(\frac{1}{L}\right)^m, \quad (4)$$

where L=128 – the number of intervals in the cycle.

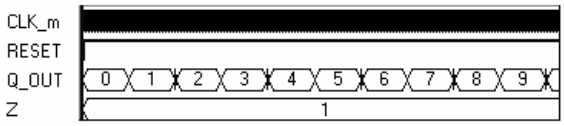

Fig. 5. Signal time graphs of the recirculator when the feedback coefficient α=0

The system reset in the initial state is performed with RESET signal, which is active when it is in the low level. At once random access memory DD3 is zeroized. If the RESET is in the high state, the module of the digital recirculator address writing and reading control DD2 is forming zero address for reading and 126th address for the writing.

The RES signal is used for the artificial synchronizing system transferring – in the mode of "synchronizing finding". This signal may be activated by the operator in the software debugging purpose. In the first place this signal activation depends on the false synchronization searching system which is in the synchronizing system consistence.

For the digital recirculator functioning verification the synchronization searching algorithm is simulated using MathCAD mathematical simulation system. The influences followed in the digital recirculator VHDL-model TESTBENCH input, are formed by the program named INFLUENCES.xmcd, which generates independent random process realizations with normal distribution of 2048 sample size. This presents one conditional cycle of the input process. The quantity of a such cycles is determined by the computer productivity. We have formed until 1000 cycles. Such a cycle is separated by m subintervals (m=16), and in the determined subinterval each cycle is add by the stable signal component multiplied by the coefficient which presents real transmitting channels characteristic. The ratio of the squared stable signal component to the squared standard deviation of the pseudo random sequence let one to set the required signal to noise level of the process in the input of the synchronizing system.

In the program, values followed from the output of the synchronizing system difference channel are saved into the text file and then are followed in the input of the TESTBENCH program. For the purpose of the testing and verification this program compares values in the output of the behavioral digital recirculator VHDL model, the results obtained by the simulation program using MathCAD (INFLUENCES.xmcd program) and post synthesis VHDL-model using CAD QUARTUS (Gate-level simulation). If the output reaction on known before correct influences of the MathCAD model are the same with VHDL-model results (post-synthesis VHDL-model) then the verification is considered as positive.

As it is known, the file type is not supported in the CAD QUARTUS, so, in the debugging, testing and verification purposes the simulation of TESTBENCH is performed in the ALDEC Active-HDL integrated environment.

The digital recirculator functioning has been debugged in the hardware using special ALTERA CYCLONE II development board. In the random access memory the phase shift keying modulated signal quadratures are loaded with sample size 2048 samples. These samples are formed in the verification system presented in [1]. These quadratures are read from the memory cyclically and are followed in the input of the programmable digital matched filter (PDMF). From its output channels the auto- and cross-correlation functions values are followed in the input of the synchronizing system which concludes the digital recirculator. The recirculator address which corresponds to the location of the mth repeated maximum of the correlation function is indicated in the seven segment indicator of the development board. Indeed, it is indicated only value equal to m when such an influence is followed in the input of programmable digital matched filter.

The style of the VHDL description is structural. Each module is presented as separate VHDL file. Each file is described using parallel operator process, and its entity is presented as component in the special package.

Conclusions

Thus, new FPGA-based digital comb filter realization using VHDL hardware description language is proposed. It increases the efficiency of spread spectrum signals synchronizing system functioning in the communication systems with code division channels. It is shown that the RAM lpm_ram_dp usage is considerably decreases the synthesis logical elements capacity of FPGA.

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ЦИФРОВИЙ РЕЦИРКУЛЯТОР НА ОСНОВІ ПЛІС

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Розглядається реалізація цифрового рециркулятора на основі ПЛІС, призначеного для забезпечення синхронізації складних сигналів в системах зв'язку з кодовим розділенням каналів при невеликих відношеннях сигнал/завада після стиску у цифровому узгоджуваному фільтрі, що програмується. VHDL-модуль представлений на рівні регістрових передач, імплементований у ПЛІС FPGA ALTERA CYCLONE II EP2C70F672C6 з використанням САПР QUARTUS. Запропоновані путі скорочення логичної ємності ПЛІС, що використовується.

Ключові слова: кодове розділення, ПЛІС, рециркулятор, синхронізація, складні сигнали.

ЦИФРОВОЙ РЕЦИРКУЛЯТОР НА ОСНОВЕ ПЛИС

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Рассматривается реализация цифрового рециркулятора на основе ПЛИС, предназначенного для обеспечения синхронизации сложных сигналов в системах связи с кодовым разделением каналов при малых отношениях сигнал/шум после сжатия в цифровом согласованном фильтре. VHDL-модуль представлен на уровне регистровых передач, представленный на уровне регистровых передач, имплиментирован в ПЛИС FPGA ALTERA CYCLONE II EP2C70F672C6 с использованием САПР QUARTUS. Предложены пути сокращения используемой логической ёмкости ПЛИС.

Ключевые слова: кодовое разделение, ПЛИС, рециркулятор, синхронизация, сложные сигналы.

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